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Design of a wideband HVDC reference divider

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***Abstract* — This paper describes design principles of a wideband HVDC reference divider. The modular divider will be used for traceable calibration of HVDC measuring systems up to 1000 kV in customers' laboratories. The first priority in the design was the accuracy of HVDC measurements. In addition the divider was designed to have wide bandwidth, both to enable measurement of ripple voltages and to prevent damage during possible flashovers.**

***Index Terms* — Measurement techniques, measurement uncertainty, voltage measurement, HVDC transmission, high-voltage techniques.**

I. INTRODUCTION

Increasing transmission voltages in high voltage d.c. (HVDC) has accentuated the need for traceable calibrations of d.c. line voltage at levels above a few 100 kV. The application requires very good accuracy for d.c., but also good response to voltages with signal components up to a several kHz. Precision HVDC dividers are traditionally based on a resistive design, whereas high voltage a.c. (HVAC) dividers from 50 Hz and above typically rely on a capacitive or a transformer design. Owing to high resistance inherent in the d.c. dividers, going from d.c. to even very low frequency (VLF) a.c. will usually lead to problems related to stray capacitances.

The experience from lightning impulse voltage (LI) reference divider design can be applied also to wideband d.c. dividers. One resistive LI divider approach is based on non-linear high voltage resistance distribution [1], [2] and another on field grading using additional electrodes [3] - [5]. The latter approach is chosen for more detailed study in this paper. Field grading has been used to extend the frequency range also on some earlier designs of reference d.c. dividers [6], but not on 1000 kV level [7].

II. ELECTRICAL CONNECTION

The system consists of two parallel dividers according to Fig. 1. A capacitive shield divider surrounds the resistive reference divider. The fast capacitive divider, made of dry polypropylene capacitors, has parallel bleeding resistor to ensure good d.c. behavior. The estimated bandwidth of the shield divider extends to tens kHz. Care has been taken to minimize the inductance of the high capacitance low voltage part of the shield divider. The response of the reference divider will follow closely the wide-band response of the shield divider.

According to simulations, a risetime of the order of 1 µs to 10 µs is attainable for the 1000 kV system [8]. The resistive current at nominal voltage is 100 µA for both shield and reference dividers, which leads to total power dissipation of 200 W for the complete divider.

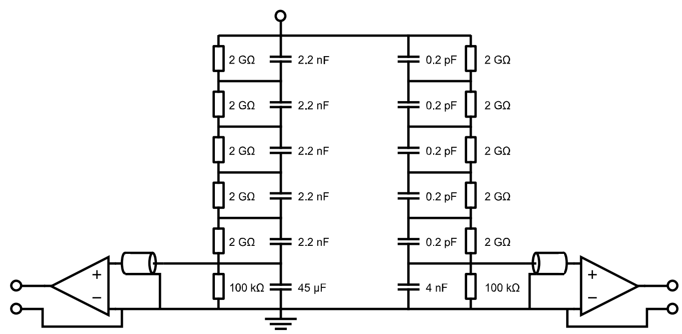

Fig. 1 Simplified schematic diagram of divider connections. Approximate component values for the shield divider shown in left, and for the reference divider on the right. The shield divider is composed of three parallel branches, which surround the reference divider.

III. STRUCTURE OF THE DIVIDER

The 1000 kV divider is sectioned in 200 kV modules. These modules will also be used separately as 200 kV dividers by the project participants. Each module is 40 cm in diameter and 1.5 m high. The modules are stackable. The design of the module is shown in Fig. 2.

Each module has a fiberglass tube as support insulator, and it will be filled with pressurized SF_6 (c. 1.5 bar). The sealed structure will ensure that the internal insulation surfaces will stay clean, and using a low pressure will provide the advantages SF_6 without ruling out possibility for air transport. The top endplate houses a gas valve, pressure gauge and a feed through for the reference divider signal. The bottom plate has a mating feed through, so that the modules can directly be stacked and mounted together.

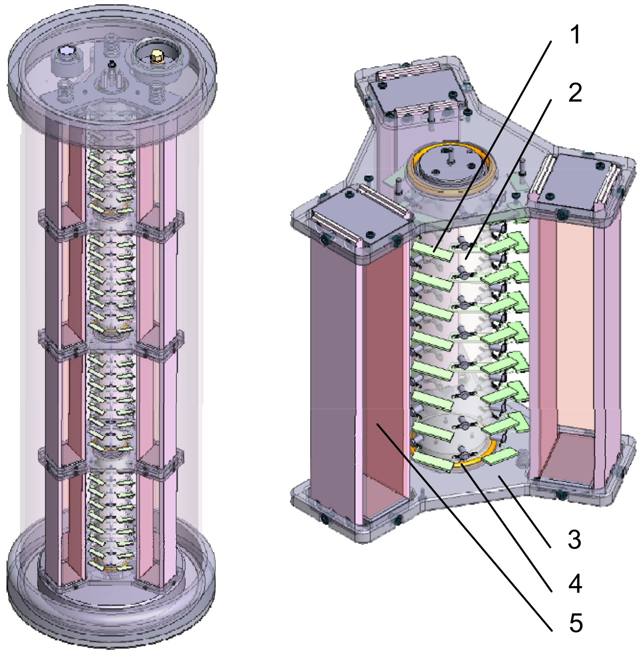

Fig. 2. Design of 200 kV module (left) and close up of a 50 kV submodule (right)

Each 200 kV module consists of four 50 kV submodules. A submodule has 51 selected 10 MΩ precision film resistors with an average temperature coefficient (TC) less than (+1.1 ± 0.2) μΩ/Ω/K., and a voltage coefficient (VC) of (-10 ± 4) μΩ/Ω/kV [9]. The low TC will reduce the effect of self heating; the known VC is easy to compensate numerically.

The resistors (green, 1) are mounted on ceramic glass (MACOR) support (light grey, 2). MACOR was selected because of its high dielectric constant ($\varepsilon_r \approx 6$) and low dielectric absorption properties; it will provide a good quality parallel capacitor for the reference resistor chain. MACOR support is insulated from the shield divider electrodes (dark grey, 3) by silicon o-rings (orange, 4). Each submodule has three dry polypropylene capacitor modules (pink, 5) around the reference resistor chain. The figure shows only the fiberglass mounting for the capacitors. These capacitors will provide both field grading for the divider and mechanical rigidity for the module internal structure.

IV. Electric field grading

The stray capacitance from the module to ground will depend on its location in the final 1000 kV stack. It was not practical to increase the shield divider capacitance to a level where the difference in ground capacitance would not affect the high frequency response of the divider. To compensate for ground capacitance differences the shield divider capacitance will increase with the position in the stack, so that the highest module will have c. 10% higher capacitance than the lowest. In this way a linear field distribution can be achieved.

The relatively high capacitance of the shield divider capacitor chain makes the field distribution linear along the reference resistor column in the center. Another advantage is that the need of external field electrodes is reduced.

V. Conclusion

We have presented the design of a divider for high accuracy d.c. measurements. Placing a wide-band shielding divider around a high-ohmic resistive divider, the bandwidth of the latter can be significantly enhanced. The film resistors selected for the design have a TC below (+1.1 ± 0.2) μΩ/Ω/K., and a voltage coefficient of (-10 ± 4) μΩ/Ω/kV. The simulations hint that with careful design the bandwidth of the 1000 kV divider under design can be in the range of tens of kilohertz, at the same time with precision of d.c. voltage measurement below 100 μV/V. Further work will be pursued with the aim to manufacture and characterize a number of divider modules for most accurate HVDC calibration work.

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